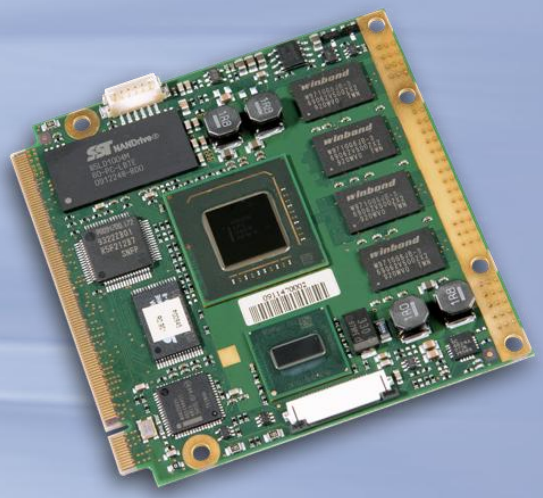
User's Manual



Q7-US15W-FD

MSC Qseven™ Module

Rev. 0.91
March 21th, 2011

Preface

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If the information provided there does not solve your problem, please contact our Technical Support:

Email: support.boards@msc-ge.com

Phone: +49 8165 906-200

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1. General Information

1.1 Revision History

Rev.	Date	Description
0.1	Jan 18th 2010	Initial version, based on MSC_Q7-US15W_User_Manual.doc
0.2	Jan 18th 2010	Minor changes
0.3	Feb 26th,2010	Bios part updated according to Bios V2.00. Added PCI IRQ routing table.
0.4	Mar 2nd 2010	Minor corrections
0.5	Mar 12th 2010	SSD Modell Number added
0.6	July 23rd 2010	Updated Bios chapter
0.7	August 3rd 2010	Minor corrections
0.8	September 1st 2010	Layout changes, minor corrections
0.9	September 7th 2010	Formatting
0.91	March 21th 2011	Block Diagram change chapter 2.2 (changed EDID EEPROM to SPD EEPROM)

1.2 Reference Documents

[1] Qseven Specification
Revision 1.11
Last update: Nov. 26th 2008

[2] PCI Local Bus Specification Rev. 2.1
PCI21.PDF
Last update: June 1st, 1995
http://www.pcisig.com

[3] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
http://www.sata-io.org/

[4] IEEE Std. 802.3-2002
802.3-2002.pdf
http://www.ieee.org

[5] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
http://www.usb.org

1.3 Introduction

Qseven modules are compact, highly integrated Single Board Computers.

Typically a Qseven module consists of CPU, chipset, memory, Ethernet controller,

BIOS flash, SATA- and USB controller. Interface controllers (e.g. for PCMCIA) or connectors (e.g. RJ45) are implemented on a base board on to which the Qseven module can be mounted.

In addition to the power supply PCIe, SATA, USB, LPC etc. interfaces are present on the connector.

Thanks to the standardized mechanics and interfaces the system can be scaled arbitrarily. Despite the modular concept the system design is very flat and compact.

Qseven modules require a base board to build a working system. For evaluation purposes MSC recommends the official Qseven Reference Platform MSC Q7-MB-RP.

2 Technical Description

2.1 Key features

Core:

Processors:
Intel Atom Z510 (1.1 GHz) or Intel Atom Z530 (1.6 GHz)

Chipset:
Intel US15W

Memory:
DDR2 400/533Mhz, soldered on module
512MB or 1GB

PCI Express Interface:
One PCIe x1 channel

Video:
Chipset integrated Graphics Media Accelerator 500
18-24 bpp single channel LVDS
1x SDVO

Ethernet:
1x 10/100/1000 Base –T LAN

Audio:
High-Definition Audio

USB:
8x USB Ports (6x USB 1.1/2.0, 2x USB 2.0 only ports, optional 1x USB Client)

I2C Bus
100kHz speed only.

SMBus

LPC Bus

SATA/PATA SSD
1x SATA port
Optional 1xPATA SSD with 4GB Memory SST85LP1004A

SDIO:

8 bit SDIO port (SDIO1.1 supported using 4 bit protocol)

BIOS:

Phoenix SecureCore BIOS with optional TPM support.

Supports FWH on base board or on module.

EEPROM:

A SMBus EEPROM is implemented for backup of the CMOS data including user BIOS setup.

Realtime Clock:

A RTC (integrated in US15W chipset) is available.

Watchdog

- Watchdog with programmable time-out
- Watchdog enabled via BIOS or application programs

System Monitoring:

Monitored values:

- Temperatures (CPU and Board)
- CPU and system fan speed

Fan support:

Optional connector on module to run active cooling fan or system fan.

Speed control via monitoring device.

TPM:

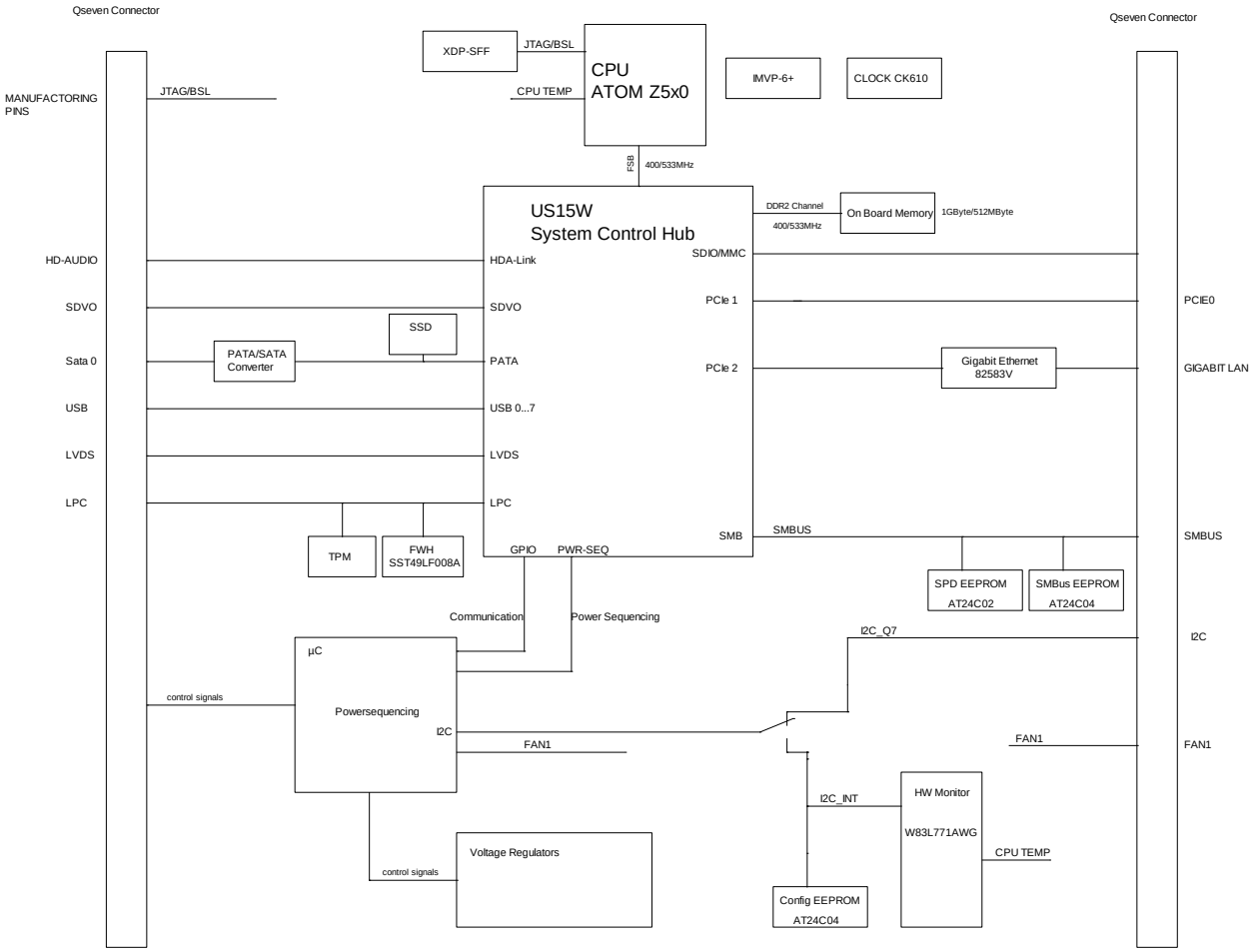
Optional Infineon TPM 1.2

2.1.1 Ordering information

Ordering number	*Part name*	*CPU*	*SSD*	*TPM*	*Memory*
32456	Q7-US15W-001	Z510	NO	NO	512MB
32457	Q7-US15W-002	Z530	NO	NO	1GB
32128	Q7-US15W-003	Z510	4GB*)	YES	1GB
32458	Q7-US15W-004	Z530	4GB*)	YES	1GB

*) Solid State Disk SSD85LP1004A

2.2 Block diagram



MSC-Q7-US15W-FD

SSD Flash depends on the Module type used.

2.3 Power Supply

- **+5V primary power supply input**
- **+5V standby**
- **3.3V RTC power supply**
  BIOS SETUP data is stored in a non volatile backup memory device (EEPROM), therefore configuration data will be retained during RTC-Power loss (except for time and date information)

Voltage	Input range	Current
+5V	+4.75V - 5.25V	See next table
+5V Standby	+4.75V - 5.25 V	
+3V RTC power supply	+2.0V - 3.3V	ca. 4uA/ max 6uA

2.4 Power dissipation

CPU: 1.1GHz
Ram: 1GByte

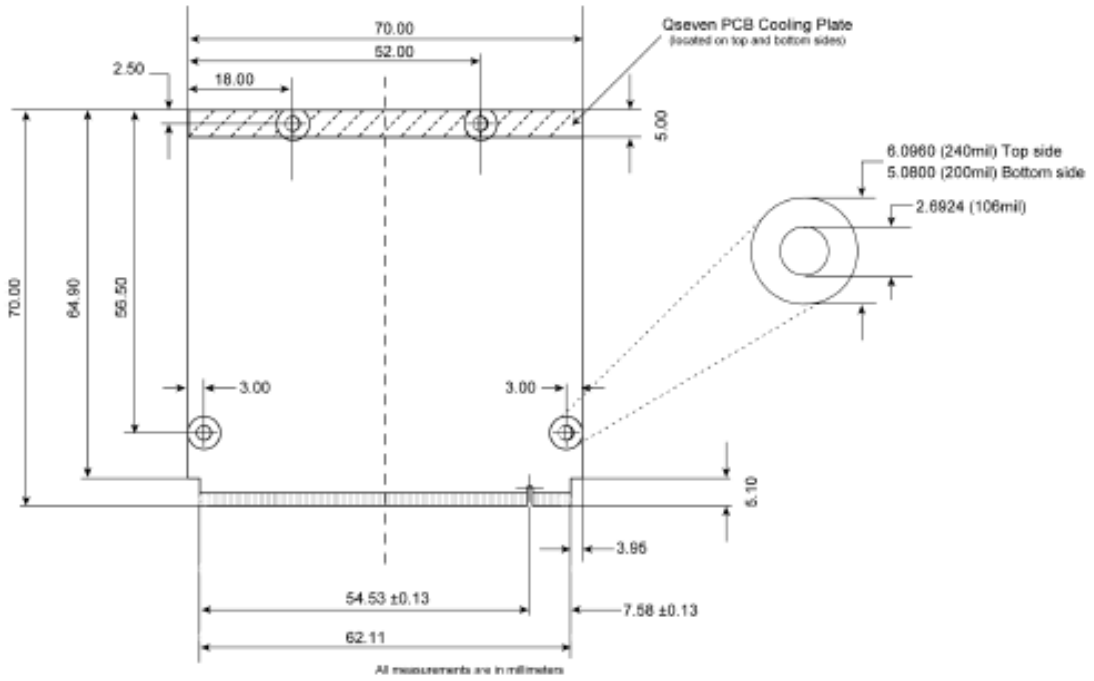
Testsoftware: Performance Test

		Idle	Calculation	Memory	Graphic	Graphic
		Idle	Find prime Number	Block read	2D Graphic complex test	3D Graphic complex test
DOS		3,6W				
Windows	S0	3,2W	4,1W	3,6W	4,5W	4,5W
	S3	0,5W				

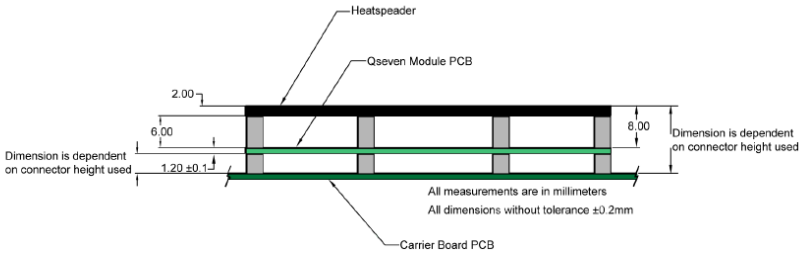
CPU: 1.6GHz
Ram: 1GByte

		Idle	Calculation	Memory	Graphic	Graphic
		Idle	Find prime number	Block read	2D Graphic complex test	3D Graphic complex test
DOS		7,2W				
Windows	S0	4,8W	5,3W	5,6W	6W	6,6W
	S3	0,5W				

2.5 Mechanical Dimensions



Qseven Module Top Side



The height is dependent on the connectors used on the baseboard.

2.6 Thermal specifications

The cooling solution for a QSeven module is based on a heatspreader concept.

A heatspreader is a metal plate (typically aluminium) mounted on top of the module. The connection between this plate and the module components is typically made using thermal interface materials such as phase change foils, gap pads and copper or aluminium blocks. A very good thermal conductivity is required in order to transfer the heat from the cpu and the chipset to the heatspreader plate.

The heatspreader used by the MSC module is thermally attached using phase change materials and small aluminium blocks filling the gap between cpu and chipset dies and heatspreader plate.

The heatspreader is not a heatsink! It is a defined thermal interface for the system designer with fixed mechanical dimensions, so it should be possible to use different module types without problem. There must be a cooling solution for the system, the surface temperature of the heatspreader should not exceed 60°C

The main goal for the thermal design of a system is that each device on the module is operated within its specified thermal limits. The max temperature of CPU and chipset are 90°C, so there may be system implementations where the heatspreader temperature could be higher.In such a case the cooling solution design should be validated such that the thermal specifications of all the components on the module are not violated across the system operating temperature range even under worst case conditions.

2.7 Signal description

In the following tables signals are marked with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different.

An additional label, "Suspend", indicates that the pin is active during suspend states (S3, S4, S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

2.7.1 High Definition Audio

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
HDA_RST#	Output	CMOS	Core	3.3V		Reset output to CODEC, active low.	US15W
HDA_SYNC	Output	CMOS	Core	3.3V		48kHz fixed-rate, sample-synchronization signal to the CODEC(s).	US15W
HDA_CLK	Output	CMOS	Core	3.3V		24.00 MHz serial data clock	US15W
HDA_SDO	Output	CMOS	Core	3.3V		Serial TDM data output to the CODEC.	US15W
HDA_SDI	Input	CMOS	Core	3.3V		Serial TDM data inputs from up to 3 CODECs.	US15W

2.7.2 Ethernet

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	Input/ Output	Analog	3.3V Sus			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. MDI[0]+/- B1_DA+/- MDI[1]+/- B1_DB+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	82574
GBE0_ACT#	Open Drain	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	Microcontroller
GBE0_LINK#	Open Drain	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 link indicator, active low.	Microcontroller

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_LINK100#	Open Drain	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	Microcontroller
GBE0_LINK1000#	Open Drain	CMOS	3.3V Sus	3.3V		Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	Microcontroller
GBE0_CTREF	REF			GND min 3.3V max		82574 (1000MBit) : 1,9V	82574

2.7.3 Serial ATA

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD	Description	Source / Target
SATA0_TX+ SATA0_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	JMH330
SATA0_RX+ SATA0_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	JMH330
SATA_ACT#	O	CMOS	3.3V	3.3V		SATA activity indicator, active low.	JMH330

2.7.4 PCI Express Lanes

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PCIE_TX[0]+ PCIE_TX[0]-	O	PCIe	Core	AC coupled on module		PCI Express Differential Transmit Pairs 0	US15W
PCIE_RX[0]+ PCIE_RX[0]-	I	PCIe	Core	AC coupled off module		PCI Express Differential Receive Pairs 0	US15W

2.7.5 USB

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
USB[0:7]+ USB[0:7]-	I/O	USB	3.3V Sus	3.3V		USB differential pairs, channels 0 through 7	US15W
USB_0_1_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	US15W
USB_2_3_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	US15W
USB_4_5_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	US15W
USB_6_7_OC#	I	CMOS	3.3V Sus	3.3V	10k PU	USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	US15W
USB_CL_PRES	I	CMOS	3.3V Sus	3.3V	10k PU	USB external Host present pin	US15W
USB_HC_SEL	I	CMOS	3.3V Sus	3.3V	100k PD	USB Host control select pin	US15W

2.7.6 LVDS Flat Panel

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LVDS_A[0:3]+ LVDS_A[0:3]-	O	LVDS	Core			LVDS Channel A differential pairs	US15W
LVDS_A_CK+ LVDS_A_CK-	O	LVDS	Core			LVDS Channel A differential clock	US15W
LVDS_PPEN	O	CMOS	Core	3.3V		LVDS panel power enable	US15W
LVDS_BLEN	O	CMOS	Core	3.3V		LVDS panel backlight enable	US15W
LVDS_BKLT_CTRL	O	CMOS	Core	3.3V		LVDS panel backlight brightness control	US15W
LVDS_BLC_CLK	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C clock output for external SSC clock chip use	US15W
LVDS_BLC_DAT	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C data line for external SSC clock chip use	US15W
LVDS_DID_CLK	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C clock output for LVDS display use	US15W
LVDS_DID_DAT	I/O OD	CMOS	3.3V	3.3V	10k PU	I2C data line for LVDS display use	US15W

2.7.7 LPC Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LPC_AD[0:3]	I/O	CMOS	Core	3.3V	20k PU	LPC multiplexed address, command and data bus	US15W
LPC_FRAME#	O	CMOS	Core	3.3V		LPC frame indicates the start of an LPC cycle	US15W
LPC_LDRQ#	I	CMOS	Core	3.3V	10k PU	LPC serial DMA request, not supported	US15W
SERIRQ	I/O	CMOS	Core	3.3V	10k PU	LPC serial interrupt	US15W
LPC_CLK	O	CMOS	3.3V	3.3V		LPC clock output - 33MHz nominal	US15W

2.7.8 SDVO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDVO_RED+ SDVO_RED-	O	PCIe		AC coupled on module		Serial Digital Video red output differential pair	US15W
SDVO_GREEN+ SDVO_GREEN-	O	PCIe		AC coupled on module		Serial Digital Video green output differential pair	US15W
SDVO_BLUE+ SDVO_BLUE-	O	PCIe		AC coupled on module		Serial Digital Video blue output differential pair	US15W
SDVO_BCLK+ SDVO_BCLK-	O	PCIe		AC coupled on module		Serial Digital Video clock output differential pair.	US15W
SDVO_INT+ SDVO_INT-	I	PCIe		AC coupled off module		Serial Digital Video interrupt input differential pair.	US15W
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I	PCIe		AC coupled off module		Serial Digital Video TVOUT synchronization clock input differential pair, not supported	US15W
SDVO_FLDSTALL+ SDVO_FLDSTALL-	I	PCIe		AC coupled off module		Serial Digital Video Field Stall input differential pair, not supported	US15W
SDVO_CTRL_CLK	I/O OD	CMOS	Core	3.3V	1M PU	SDVO I2C clock line - to set up SDVO peripherals.	US15W
SDVO_CTRL_DAT	I/O OD	CMOS	Core	3.3V	1M PU	SDVO I2C data line - to set up SDVO peripherals.	US15W

2.7.9 SDIO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDIO_DAT[0:7]	I/O	3.3V	Core	3.3V		SDIO Controller Data	US15W
SDIO_CD#	I	3.3V	Core	3.3V		SDIO Controller Card Detect	US15W
SDIO_CMD	I/O	3.3V	Core	3.3V	10k PU	SDIO Controller Command	US15W
SDIO_CLK#	O	3.3V	Core	3.3V		SDIO Controller Clock	US15W
SDIO_PWR#	I/O	3.3V	Core	3.3V		SDIO Controller Power enable	US15W
SDIO_LED	O	3.3V	Core	3.3V		SDIO Controller transfer activity LED	US15W
SDIO_WP	I	3.3V	Core	3.3V		SDIO Controller Write Protect	US15W

2.7.10 Express card support

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
EXCD0_CPPE#	I	3.3V	Core	3.3V		Express card slot 0 card request	Microcontroller
EXCD0_PERST#	O	3.3V	Core	3.3V		Express card slot 0 reset	Microcontroller
EXCD1_CPPE#	I	3.3V	Core	3.3V		Express card slot 1 card request	Microcontroller
EXCD1_PERST#	O	3.3V	Core	3.3V		Express card slot 1 reset	Microcontroller

2.7.11 Miscellaneous

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
I2C_CLK	I/O	CMOS	3.3V	3.3V	2k PU	General purpose I2C port clock output	
I2C_DAT	I/O	CMOS	3.3V	3.3V	2k PU	General purpose I2C port data I/O line	
SPKR	O	CMOS	3.3V	3.3V		Output for audio enunciator - the "speaker" in PC-AT systems	

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
BIOS_DISABLE#	I	CMOS	3.3V	3.3V	10k PU	Module BIOS disable input. Pull low to disable module BIOS.	
WDOUT	O	CMOS	3.3V	3.3V		Output indicating that a watchdog time-out event has occurred.	Microcontroller
WDTRIG#	I	CMOS	3.3V	3.3V	10k PU	Watchdog trigger input. This signal restarts the watchdog timer	Microcontroller
FAN_TACHOIN	I	CMOS	3.3V			Tachometer input	Microcontroller
FAN_PWMOUT	O	CMOS	3.3V			Pulse width modulation output for fan speed control	Microcontroller

2.7.12 Power and System Management

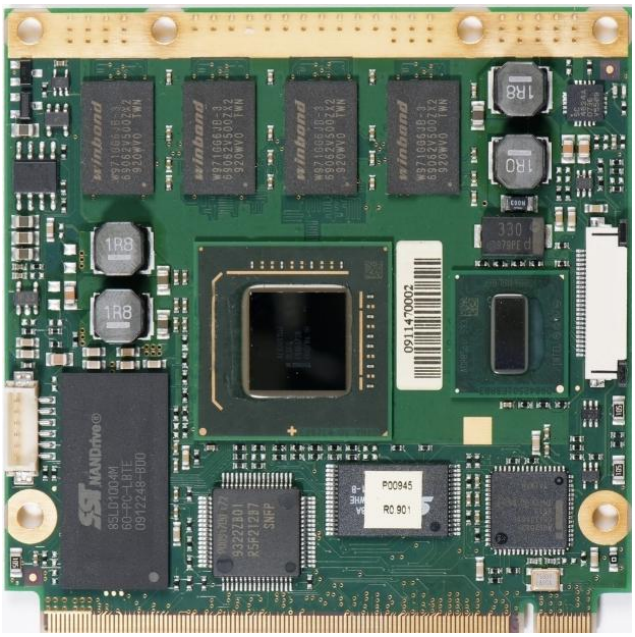
Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PWRBTN#	I	CMOS	3.3V Sus	3.3V	10k PU	Power button to bring system into a power state. (Negative pulse)	
RSTBTN#	I	CMOS	3.3V Sus	3.3V	10k PU	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release. (Negative pulse)	
SUS_STAT#	O	CMOS	3.3V Sus	3.3V		Indicates low power suspend operation	
SUS_S3#	O	CMOS	3.3V Sus	3.3V		Indicates system is in Suspend to RAM state. Active low output.	
SUS_S5#	O	CMOS	3.3V Sus	3.3V		Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	
WAKE#	I	CMOS	3.3V Sus	3.3V	10k PU	External system wake up signal.	
BATLOW#	I	CMOS	3.3V Sus	3.3V	10k PU	Indicates that external battery is low.	
THRM#	I	CMOS	3.3V	3.3V	8k2 PU	Input from off-module temp sensor indicating an over-temp situation.	
THERMTRIP#	O	CMOS	3.3V	3.3V		Active low output indicating that the CPU has entered thermal shutdown.	
SMB_CLK	I/O	CMOS		3.3V	2k PU	System management clock line	
SMB_DAT	I/O	CMOS		3.3V	2k PU	System management data line	
SMB_Alert	I/O	CMOS		3.3V	10k	System management bus alert input	
SLP_BTN#	I	CMOS		3.3V Sus	10k PU	Sleep button. Low active signal to bring the system in sleep state. (Negative pulse)	

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LID_BTN#	I	CMOS		3.3V Sus	10k PU	LID button. Low active signal detect a LID switch to bring the system in sleep state or wake up again.(Low signal)	
BATLOW#	I	CMOS		3.3V Sus	10k PU	Battery low input indicates a external battery low state	
PWGIN	I	Low<0.6V High>0.8V		5V	120k PD	Indicates that the external power supply is ready	

2.7.13 Power and GND

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VCC_5V	Power		5V (±5%)			Primary power input: +5V (±5%)	Voltage Regulators
VCC_5V_SBY	Power		5V (±5%)			Standby power input: +5.0V (±5%) All available VCC_5V_SBY pins on the connector(s) shall be used. Used for microcontroller and standby and suspend functions. If no standby power is available connect to VCC_5V	VCC3.3V SUS regulator
VCC_RTC	Power					Real-time clock circuit-power input : +3.0V (+2.0V to +3.3V)	
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.8 Connectors



2.8.1 Module connector

Row A		Row B	
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
KEY		KEY	
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE#	42	SDIO_CLK#

43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	NC
57	GND	58	GND
59	HDA_SYNC	60	SMB_CLK
61	HDA_RST#	62	SMB_DAT
63	HDA_BITCLK	64	SMB_ALERT#
65	HDA_SDI	66	I2C_CLK
67	HDA_SDO	68	I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7-	76	USB_P6-
77	USB_P7+	78	USB_P6+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5-	82	USB_P4-
83	USB_P5+	84	USB_P4+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CL_PRES	92	USB_HC_SEL
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	LVDS_A0+	100	NC
101	LVDS_A0-	102	NC
103	LVDS_A1+	104	NC
105	LVDS_A1-	106	NC
107	LVDS_A2+	108	NC
109	LVDS_A2-	110	NC
111	LVDS_PPEN	112	LVDS_BLEN
113	LVDS_A3+	114	NC
115	LVDS_A3-	116	NC
117	GND	118	GND
119	LVDS_A_CLK+	120	NC
121	LVDS_A_CLK-	122	NC
123	LVDS_BLT_CTRL	124	RSVD
125	LVDS_DID_DAT	126	LVDS_BLC_DAT
127	LVDS_DID_CLK	128	LVDS_BLC_CLK
129	RSVD	130	RSVD

131	SDVO_BCLK+	132	SDVO_INT+
133	SDVO_BCLK-	134	SDVO_INT-
135	GND	136	GND
137	SDVO_GREEN+	138	SDVO_FLDSTALL+
139	SDVO_GREEN-	140	SDVO_FLDSTALL-
141	GND	142	GND
143	SDVO_BLUE+	144	SDVO_TVCLKIN+
145	SDVO_BLUE-	146	SDVO_TVCLKIN-
147	GND	148	GND
149	SDVO_RED+	150	SDVO_CTRL_DAT
151	SDVO_RED-	152	SDVO_CTRL_CLK
153	NC	154	NC
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	EXCD0_PERST#	172	EXCD1_PERST#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	EXCD0_CPPE#	178	EXCD1_CPPE#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	LPC_CLK	190	LPC_FRAME#
191	SERIRQ	192	LPC_LDRQ#
193	VCC_RTC	194	SPKR
195	FAN_TACHOIN	196	FAN_PWMOUT
197	GND	198	GND
199	RSVD	200	RSVD
201	RSVD	202	RSVD
203	RSVD	204	RSVD
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC

219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

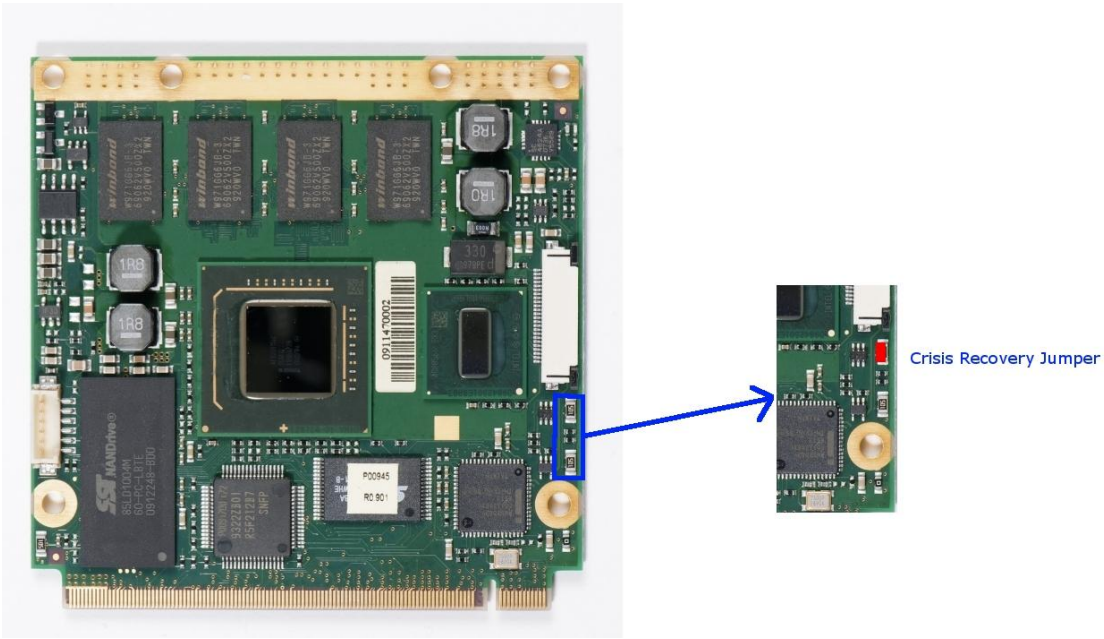
3 Jumpers

3.1 Crisis recovery jumper

If a bios crisis recovery is necessary the crisis recovery jumper can be shorted across R0901 with a small tweezers and press the reset button. After the crisis beep the tweezers can be removed.

Note: ***R0901 is connected to +3,3V so be aware that the tweezers do not touch the heat spreader or any other electronic component on the board. The board could otherwise be damaged.***

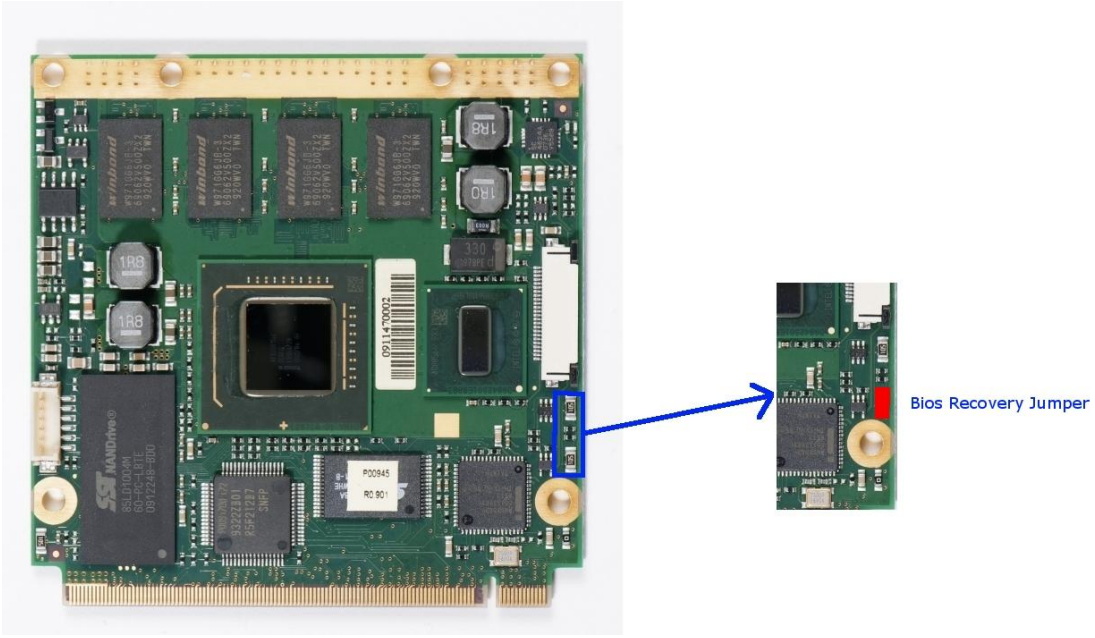
Please see also the bios recovery procedure described in the ***bios crisis recovery*** section.



3.2 Clear CMOS jumper

To clear the CMOS memory, short the resistor R0905 with a small pair of tweezers and press the reset button.

Note: R0905 is connected to +3,3V so be aware that the tweezers must not touch the heat spreader or any other electronic component on the board. The board could otherwise be damaged.



4 System resources

4.1 SMB Address Map

Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
ICS9UMS9610 Clock Synthesizer	1	1	0	1	0	0	1	x	D2h / 69h
CMOS backup EEPROM	1	0	1	0	1	0	0	x	A8h / 54h
SPD EEPROM (SO-DIMM)	1	0	1	0	0	0	0	x	A0h / 50h

*) 8 bit address (with R/W) / 7 bit address (without R/W)

4.2 PCI Express Lanes

Signal /Slot	Source
PCIE_TX[0] PCIE_RX[0]	PCIe-Channel 1 US15W

4.3 USB

Signal	Source / Target	Remark
USB[0]+ USB[0]-	USB0 US15W	USB1.1/2.0
USB[1]+ USB[1]-	USB2 US15W	USB1.1/2.0 (Optional client,Chipset port 2)
USB[2]+ USB[2]-	USB1 US15W	USB1.1/2.0 (Chipset port 1)
USB[3]+ USB[3]-	USB3 US15W	USB1.1/2.0
USB[4]+ USB[4]-	USB4 US15W	USB1.1/2.0
USB[5]+ USB[5]-	USB5 US15W	USB1.1/2.0
USB[6]+ USB[6]-	USB6 US15W	USB2.0
USB[7]+ USB[7]-	USB7 US15W	USB2.0

4.4 PCI Devices

Qseven			Interrupts of Controller (US15W)							
Slot Number (or Onboard Device)	**IDSEL # or DEV. #**	**Bus #**	**PIRQ 0 (INT A)**	**PIRQ 1 (INT B)**	**PIRQ 2 (INT C)**	**PIRQ 3 (INT D)**	**PIRQ 4 (INT E)**	**PIRQ 5 (INT F)**	**PIRQ 6 (INT G)**	**PIRQ 7 (INT H)**
Internal Graphic Device	Dev 02h	0					A			
USB Client Controller	Dev 26 Fkt 0	0							A	
HD Audio	Dev 27 Fkt 2	0					A			
PCI Express Root Port	Dev 28 Fkt 0/1	0	B	A						
USB UHCI Host Controller	Dev 29 Fkt 0	0								A
USB UHCI Host Controller	Dev 29 Fkt 1	0							B	
USB UHCI Host Controller	Dev 29 Fkt 2	0							C	
USB EHCI Controller	Dev 29 Fkt 7	0						D		
SDIO	Dev 30 Fkt 0/1/2	0					A/B /C			
SATA (optional)	Dev ? Fkt 0	-			A					
GB Lan Controller (optional)	Dev ? Fkt 0	-		A* (NO switch)		A* (switch)				
PCIe Slot 1 (optional)	Dev ? Fkt 0	-	A	B	C	D				
PCIe Slot 2 (optional)	Dev ? Fkt 0	-	D	A	B	C				
PCIe Slot 4 (optional)	Dev ? Fkt 0	-	C	D	A	B				

*) Routing for GB Lan Controller depends on how it is connected to PCIe bus (device directly connected to PCIe root port or behind PCIe switch).

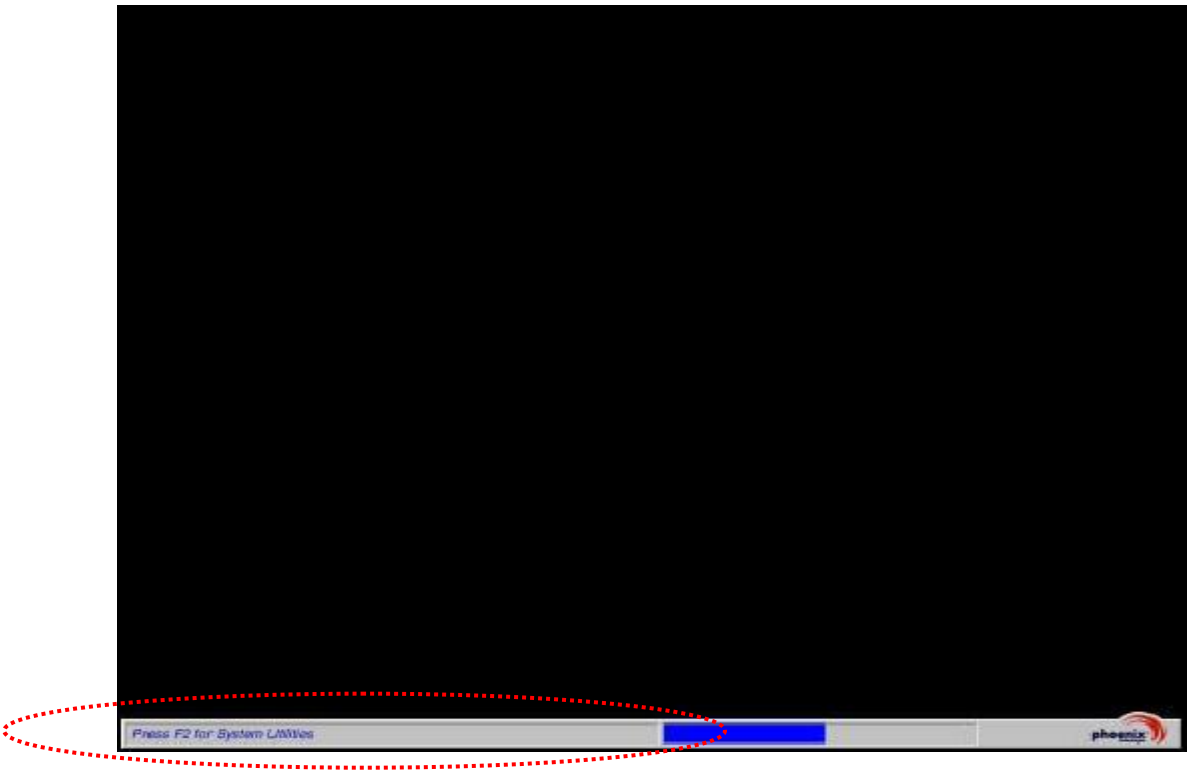
5 BIOS

5.1 Introduction

This guide describes the Phoenix TrustedCore Startup screen and contains information on how to access Phoenix TrustedCore setup to modify the settings which control Phoenix pre-OS (operating system) functions.

5.1.1 Startup Screen Overview

The Phoenix TrustedCore Startup screen is a graphical user interface (GUI) that is included in Phoenix TrustedCore products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen, including a progress bar at the bottom of the screen. This bar indicates the progress of the Startup Screen functions and provides user prompting and POST status. The following figure shows the various parts of a generic Startup Screen at 1024x768 resolution:



5.1.2 Activity Detection Background

While the Startup screen is displayed, press the Setup Entry key (F2 – TrustedCore default). The Startup Status Bar acknowledges the input, and at the end of POST, the screen clears and setup launches.
An example of the Startup Status Bar displaying changing state is shown in the following figure. The "Please Wait…" text is displayed after the F2 key is pressed to acknowledge user input.

Active status bar:

5.2 TrustedCore Setup Utility

With the Phoenix TrustedCore Setup program, you can modify TrustedCore settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

5.2.1 Configuring the System BIOS

To start the Phoenix TrustedCore Setup utility, press [F2] to launch Setup. The Setup main menu appears.

The BIOS Menu Structure

The BIOS Menu is structured in the following way:

Main		
	Board Information	
	Primary Master	
	Primary Slave	
	Keyboard Features	
	Boot Options	
Advanced		
	Cache Memory	
	Atom CPU Control Sub-Menu	
		CPU Thermal Control Sub-Menu
	Chipset Control Sub-menu	
		PCI Express Control Sub-Menu
		US15W USB Control Sub-Menu
	Video (Intel IGD) Control Sub-Menu	
	I/O Device Configuration	
	ACPI Control Sub-Menu	
	Watchdog Options	
Security		
Power		
	Hardware Monitor	
Boot		
Exit		

The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu Items	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Security	Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders.
Power	Use this menu to configure Power-Management features.
Boot	Use this menu to set the boot order in which the BIOS attempts to boot to OS.
Exit	Exits the current menu.

Use the left and right arrow keys on your keyboard to make a menu selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom of the screen to make your selections, or to exit the current menu. The following table describes the legend keys and their alternates:

Key	Function
F1 or Alt-H	General Help window.
Esc	Exit this menu.
Arrow keys	Select a different menu.
Up and down arrow keys	Move cursor up and down.
Tab or Shift-Tab	Move cursor left and right (i.e. at System Time / System Date).
Home or End	Move cursor to top or bottom of window.
PgUp or PgDn	Move cursor to next or previous page.
F5 or -	Select the previous value for the field.
F6 or + or Space	Select the next value for the field.
F9	Load the Default Configuration values (for all menus).
F10	Save and exit.
Enter	Execute command or select submenu.

Select an item

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

Display a submenu

To display a submenu, use the arrow keys to move the cursor to the sub menu you want. Then press Enter. A pointer marks all submenus.

5.2.2 The Main Menu

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
Board Information	Submenu	Displays BIOS Version
System Time	Enter Time (HH:MM:SS)	Set the System Time.
System Date	Enter Date (DD/MM/YYYY)	Set the System Date.
Keyboard Features	Submenu	Configure Keyboard Options
Boot Options	Submenu	Configure Boot Options

5.2.2.1 Board Information

Feature	Options	Description
HW Platform	Informative	Name of the hardware platform
HW Revision	Informative	Hardware revision number
Bios Version	Informative	Shows current bios version.
Serial #	Informative	Hardware Serial Number
MAC Address	Informative	Internal Lan Mac Adress
Boot Counter	Informative	The number of times this board has booted up.
CPU String	Informative	CPU Identification string
CPU Speed	Informative	CPU Speed
CPU Class	Informative	CPU ID Class code
CPU Model	Informative	CPU ID Model code
CPU Stepping	Informative	CPU ID Stepping
CPU Cores	Informative	Number of CPU cores
Microcode Patch ID	Informative	Microcode Patch ID
EC HW Name	Informative	Embedded Controller Hardware Name
EC HW Version	Informative	Embedded Controller Hardware Version
EC SW Name	Informative	Embedded Controller Software Version
EC SW Version	Informative	Embedded Controller software Version
System Memory	Informative	Amount of memory below 1MB
Extended Memory	Informative	Total amount of memory
UUID	Informative	Shows UUID

5.2.2.2 Keyboard Features

Feature	Options	Description
NumLock	Auto, On, Off	Selects Power-on state for NumLock
Keyclick	Enabled, Disabled	Enables Key click

Feature	Options	Description
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18.5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Selects key repeat rate
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Selects delay before key repeat

5.2.2.3 Boot Options

Feature	Options	Description
Summary screen	Disabled, Enabled	**Enabled** displays system configuration on boot.
Boot-time Diagnostic Screen	Disabled, Enabled	**Enabled** displays the diagnostic screen during boot. **Disabled** displays the Boot Logo.
Quick Boot Mode	Enabled, Disabled	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Hard Disk Pre-Delay	Disabled, 3/6/9/12/15/21/30 seconds	Adds a Delay before the first access of a hard disk by the Bios. Some hard disk hang if the have initialized before the have initialized themselves. This delay ensures the hard disk has initialized after power up, prior to being accessed.
Extended Memory Testing	Normal, Just zero it, None	Determines which type of test will be performed on extended memory during POST (above 1 MB).
Post Errors	Disabled, Enabled	Pauses and displays Setup Entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.

5.2.3 The Advanced Menu

Feature	Options	Description
Installed O/S	Other, Win95, Win98, WinMe, Win2000, WinXP	Select the operating system installed on your system which you will use most commonly. **NOTE**: An incorrect setting can cause some operating systems to display unexpected behavior.
Reset configuration Data	No, Yes	Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area.

Feature	Options	Description
Large Disk Access Mode	Other, DOS	Select **Other** for UNIX, Novell NetWare. Select **DOS** for all other operating systems.
Small LBA-Disk CHS Translation	No, Yes	Select if CHS translation should be made for a LBA-capable hard disk with less than 1024 cylinders, e.g. CompactFlash(R). If you have problems with booting from a CompactFlash(R), try to change this setting. No = translate CHS only if HDD has >1024 cyls. Yes = translate CHS for all LBA-capable disks.
On-board Lan	Enabled, Disabled	Controls Power to the onboard Device Disabled = Disables the on-board LAN device. Enabled: Enables the on-board LAN device.
PXE OPROM	Enabled, Disabled	Enable PXE Option ROM for the onboard LAN device. Note: This option is appears only if the on-board LAN device is enabled.
SDIO Controller Boot Rom	Enabled, Disabled	Enable or disable the SD Controller's Bootrom which adds support for booting from SD cards.
Cache Memory	Submenu	Configure Cache Memory
Atom CPU Control Sub-Menu	Submenu	Configure CPU Control
US15W Control Sub-Menu	Submenu	Configure MCH Control
Video (Intel IGD) Control Sub-Menu	Submenu	Configure Video (Intel IGD) Control
I/O Device Configuration	Submenu	Configure I/O Device
ACPI Control Sub-Menu	Submenu	Configure ACPI Control
CK-610 Clock Chip	Default, Programm	Control Programming of the CK-610 Clock Chip Default = Power On Default Values. Program = TBD

5.2.3.1 Cache Memory Control Menu

Feature	Options	Description
Memory Cache:	Enabled, Disabled	Sets the state of the memory cache.
Cache System BIOS area	Uncached, Write Protect	Enables caching of system BIOS area.
Cache Video BIOS area	Uncached, Write Protect	Enables caching of video BIOS area.
Cache Extended Memory Area	Uncached, Write Through, Write Protect, Write Back	Controls caching of system memory above one megabyte.
Cache D000 – D3FF Cache D400 – D7FF Cache D800 – DBFF Cache E000 – E3FFF	Disabled, Write Through, Write Protect, Write Back	**Disabled** = This block is not cached. **Write through** = Writes are cached and sent to main memory at once. **Write Protect** = Writes are ignored. **Write Back** = Writes are cached but not sent to main memory until necessary.

5.2.3.2 Atom CPU Control Sub-Menu

Feature	Options	Description
Hyperthreading	Enabled, Disabled	Enabling Hyperthreading activates additional CPU threads. These threads may appear as additional processors but will share some resources with other threads within the physical package. ***Note:*** ***Only supported by Intel Atom Z530***
Processor Power Management	Disabled, GV3 only, C-States Only, Enabled	Selects the Processor Power Management desired: Disabled = C-States and GV3 are disabled. GV3 Only = C-States are disabled. C-States Only = GV3 is disabled. Enabled = C-States und GV3 are enabled. **Note**: GV3 refers to the speed step capability of the CPU. **Note**: If GV3 is disabled, OS will not run with maximum frequency. To use maximum frequency, GV3 has to be enabled and OS must Control the CPU frequency via Power management. **Note**: For optimal response times the GV3 (Speed step) must be enabled and C-States disabled. Also disable C-States if using RS232 @ 115k baud. Otherwise receiving errors could occur.
Enhanced C-States	Enabled, Disabled	Enables Enhanced C-State support Disabled = Enhanced C-States disabled. Enabled = Enhanced C-States enabled.
Thermal Control Circuit	TM1 TM1 and TM2	Setting this bit enables the thermal control circuit (TCC) portion of the Thermal Monitor feature of the CPU. Intel Thermal Monitor TM1= 50% duty cycle TM2= Geyserville III
DTS Enable	Disabled, Enabled	Enables the Atom DTS to be used for platform Thermal Management.

Feature	Options	Description
No Execute Mode Mem Protection	Enabled, Disabled	When disabled, forces the Execute-Disable Bit Capability extended feature bit to always return 0.
Intel ® Virtualization Technology	Enabled, Disabled	Enables or disables Intel Virtualization Technology. ***Note:*** ***Only supported by Intel Atom Z530***
Set Max Ext CPUID = 3	Disabled, Enabled	Sets Max CPUID extended function value to 3.
PROCHOT# Enable	Enabled, Disabled	The processor PROCHOT# signal can be enabled for throttling. PROCHOT# is asserted by the embedded controller. To change the threshold values please contact our technical support. The CPU internal PROCHOT# generation is independent of these settings.

5.2.3.3 US15W Control Sub-Menu

Feature	Options	Description
PCI Express Control Sub-Menu	Sub-Menu	Configure PCI Express Control
PCI Control Sub-Menu	Sub-Menu	Additional setup menus to configure PCI devices.
USB Control Sub-Menu	Sub-Menu	Configure USB Control
HD Audio Controller	Disabled, Auto	Control Detection of the Azalia Device. Dev 27, Fun 0 Disabled = Azalia will be unconditionally disabled, regardless of presence. Auto = Azalia will be enabled if present, disabled otherwise.
SDIO Controller	Enabled, Disabled	Control SDIO functionality through this Setup Item. Dev 30, Fun 0/1/2

Feature	Options	Description
Pop Up Mode Enable	Disabled, Enabled	Select the proper mode: If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events. If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters.
Pop Down Mode Enable	Disabled, Enabled	Should be enabled only if Pop up is enabled: If disabled, ICH will NOT attempt to automatically return. If enabled, ICH will observe a NO bus master request and it can return to a previous C3 or C4 state.
Memory Throttling	50%, 75%, 25%, Disabled	Memory and graphics clock will be throttled to the selected memory bandwidth percentage on reaching the temperature threshold. To change the threshold values please contact our technical support.

5.2.3.4 PCI Express Control Sub-Menu

Feature	Options	Description
PCI Express – Root Port 1	Disabled, Enabled, Auto	Control PCI Express Port via this setup option. Disabled = Port always Disabled. Auto = Only enable if card found. Note that if Root Port 1 is disabled Root Port 2 will be disabled as well.
PCI Express – Root Port 2	Disabled, Enabled, Auto	Control PCI Express Port via this setup option. Disabled = Port always Disabled. Auto = Only enable if card found. Note that if Root Port 1 is disabled Root Port 2 will be disabled as well.
Root Port ASPM Support	Disabled, Auto	Control ASPM support for all the enabled Root Ports. Auto = will set APMC to the highest common supported ASPM between the Port and Endpoint.

ASPM Latency Checking	Disabled, Enabled	Disabled: ASPM latencies are ignored when enabling ASPM. Enabled: Enables ASPM latency checking when enabling ASPM.

5.2.3.5 PCI Control Sub-Menu

Feature	Options	Description
PCI IRQ Line 0	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports
PCI IRQ Line 1	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports
PCI IRQ Line 2	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports
PCI IRQ Line 3	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports
PCI IRQ Line 4	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: Internal Graphics, HD Audio, SD Card Controller
PCI IRQ Line 5	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: EHCI Controller
PCI IRQ Line 6	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: USB Client, UHCI Controller 2, UHCI Controller 3

Feature	Options	Description
PCI IRQ Line 7	Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: UHCI Controller 1

5.2.3.6 US15W USB Control Sub-Menu

Feature	Options	Description
USB 1.1 Controllers	Port 0-1 Port 0-3 Port 0-5	Select the number of enabled USB1.1 Controllers. Port 0-1 = Dev 29, Fun 0 Port 2-3 = Dev 29, Fun1 Port 4-5 = Dev 29, Fun 2 Note: Port 6-7 can only be used as USB 2.0 Port 1 in the chipset is equivalent to Port 2 on the Q7 connector. Port 2 in the chipset is equivalent to Port 1 on the Q7 connector.
USB 2.0 Ports	Disabled, Enabled	Control USB 2.0 functionality of port 0-7 through this Setup Item. Dev 29, Fun 7 Note: Port 6-7 can only be used as USB 2.0
USB Client (depends on USB_HC_SE)	Disabled, Enabled	If enabled, one USB Port 2 can be used as a Client.

5.2.3.7 Video (Intel IGD) Control Sub-Menu

Feature	Options	Description
IGD – Device 2	Disabled, Auto	Enables or Disable the Internal Graphics Device by setting item to the desired value.
IGD – Boot Type	VBIOS default, CRT, LFP, TV, EFP,	Select the Video Device that will be activated during POST.
IGD – S3 Popup	Disabled, Enabled	If the IGD is the primary display device and this option is set to enabled, a Popup Icon will be displayed for 5 seconds during ACPI S3 resume.

Feature	Options	Description
Pre-Allocated Memory Size	1 MB, 4 MB, 8 MB	Select the amount of Pre-Allocated Graphics Memory for use by the Internal Graphics Device.
IGD – LCD Panel Type	640x480 1 PPC, 18b 800x600 1 PPC, 18b 1024x768 1 PPC, 18b 640x480, 1 PPC, 18b 800x480, 1 PPC, 18b 1024x600 1 PPC, 18b 800x480 1 PPC, 24b 800x600 1 PPC, 24b 1024x768 1 PPC, 24b 1280x800 1 PPC, 24b 1366x768 1 PPC, 24b 12: Reserved 13: Reserved 1280x800, 1PPC, 18b 1280x600, 1PPC, 18b 1366x768, 1PPC, 18b	Select the LCD panel used by the Internal Graphics Device by selecting the appropriate setup item. The first item is Panel 1, the last item is Panel 16. Some Panels are not numbered due to size constraints. **Note**: Due to size constrains not all Panels are exactly numbered. The first item is Panel 1, the last one Panel 16.
IGD – Panel Scaling	Auto, Force Scaling, Off	Selects the LCD panel scaling option used by the Internal Graphics Device. 1. Auto 2. Force Scaling 3. Off
Backlight Brightness	10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%	Select the starting brightness for the LVDS backlight signal. **Note**: some backlight inverters use an inverted level for brightness control – please check the inverter spec. for the display panel

5.2.3.8 I/O Device Configuration Menu

Feature	Options	Description
Serial Port A	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port A.
Interrupt	3, 4	Set the interrupt for Serial Port A.
Serial Port B	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Mode	Normal, IR, ASK-IR	Set the mode for Serial Port B (wired / infrared).

Feature	Options	Description
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port B.
Interrupt	3, 4	Set the interrupt for Serial Port B.

Warning: If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings.

Note: Depending on type of the Super IO used it is possible to have more than 2 Com Ports selectable in this Menu.

Note: If using RS232 @ 115k baud, it is recommended to disable C-States and enable GV-3 only in CPU-Control Sub-Menu. Otherwise receiving errors could occur due to chipset and CPU related limitations.

5.2.3.9 ACPI Control Sub-Menu

Feature	Options	Description
Passive Cooling Trip Point	Disabled, 63 C, 71 C, 79 C, 87 C	This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU. Note: If the DTS is enabled, only values below 90C are valid.
Passive TC1 Value, Passive TC2 Value,	0 - 15	This value sets the TC1-2 value for the ACPI Passive Cooling Formula.
Passive TSP Value	1 - 15	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled.
Critical Trip Point	POR, 63 C, 71 C, 79 C, 87 C	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. Notes: (1)100C is POR for all Intel's CPUs. (2) If value is > 100C and DTS is enabled, the Out-of-Spec Bit will be used. (3) The EC value will be set to 127 after ACPI initialization.
FACP – RTC S4 Flag Value	Disabled, Enabled	Valid only for ACPI Control the value for the RTC S4 flag in the FACP Table

Feature	Options	Description
FACP – PM Timer Flag Value	Disabled, Enabled	Valid only for ACPI Controls the timer used by the OS through the FACP Tables Flags. This is now possible with WINXP SP2 and beyond.
HPET Support	Disabled, Enabled	This field is valid only in the Windows XP OS. Control the High Performance Event Timer through this setup option when enabled. The HPET Table will then be pointed to by the RSDT and the proper enable bits will be set.
HPET Base Address	0xFED00000, 0xFED01000, 0xFED02000, 0xFED03000	Select the Base Address for the High Performance Event Timer.

5.2.3.10 Watchdog Options

Feature	Options	Description
Watchdog delay	1 second, 5 seconds, 10 seconds, 30 seconds 1 minute , 5 minutes, 10 minutes, 30 minutes	After watchdog is activated, it waits selected delay time before it starts counting the timeout period.
Watchdog timeout	0.4 second, 1 second, 5 seconds, 10 seconds, 30 seconds, 1 minute , 5 minutes, 10 minutes	Select the maximum watchdog trigger period. If the watchdog will not be triggered during selected period, system reset will be generated.
Watchdog start on boot	No, Yes	Select if the watchdog should be started at the end of POST.

5.2.3.11 The Security Menu

Feature	Options	Description
Supervisor Password Is	Displays Supervisor Password Is	Displays the current status of the Supervisor password ("Clear" or "Set")
User Password Is	Displays User Password Is	Displays the current status of the User password ("Clear" or "Set")

Set Supervisor Password	Press return to enter supervisor password	Supervisor Password controls access to the setup utility.
Set User Password	Press return to enter user password	User Password controls access to the system at boot.
Password on boot	Disabled, Enabled	Enables password entry on boot
TPM support	Disabled, Enabled	Enable Trusted Platform Module support
Current TPM State	Informative	Show the current TPM State
Change TPM State	No Change, Enable & Activate , Deactivate and Disable, Clear	Changes TPM State

5.2.4

5.2.4 The Power Menu

Feature	Options	Description
After Power Failure	Power On, Off	Sets the mode of operation if an AC Power Loss occurs.
Power Button Wake	Always, S4/S5 only	This item controls from which sleep state the Power Button shall wake the system. Always – from S3, S4 and S5 S4/S5 only – from S4 and S5
Sleep Button Wake	S3 only, Off	This item controls from which sleep state the Sleep Button shall wake the system. S3 – from S3 only
Wake Signal	Off, S3 only, S4/S5 only, Always	This item controls from which sleep state the Wake signal shall wake the system. Off – Never S3 – from S3 only S4/S5 only – from S4 and S5 Always – from S3, S4 and S5
Lid Switch Wake	S3 only, Off	This item controls from which sleep state the Lid Switch shall wake the system. Off – Never S3 – from S3 only
Lid Switch Polarity	Standard, Inverted	Lid state (Standard): High = opened, Low = closed Lid state (Inverted): High = closed. Low = opened
Hardware Monitor	Submenu	Configure Hardware Monitor

Note: All features of the Power Menu with exception for Power Button Wake are without function on modules with Hardware Revision 2.

5.2.4.1 Hardware Monitoring Menu

Feature	Description
CPU Temperature Sensor	Displays the current CPU temperature.
Local Temperature	Displays the current local temperature on the bottom side near the RAM.
Fan Speed	Shows Fan Speed

5.2.5 The Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as DOS, Windows XP or Linux) from a device listed in the boot priority order. If it cannot find the operating system on that device, it will attempt to load it from the next device in that list. Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g. USB sticks), and network cards.

Note: Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Feature	Description
Boot priority order: 1: USB KEY: 2: USB HDD: 3: USB CDROM: 4: PCI SCSI: 5: PCI BEV: 6: 7: 8:	Boot priority order for next boot. System tries to boot the first bootable device in this list. Use <+> and <-> to change order. Use <x> to exclude or include device to boot priority list.
Exclude from boot order: : USB FDC:	System does not try to boot a device from this list.

Pressing the "F10" key during the bios boot phase will bring up the bios boot menu, which will allow you to select a different boot device for the current boot process only. In this boot menu, only devices in the "Boot priority list" will selectable. Devices excluded from boot order will not be shown.

5.2.6 The Exit Menu

The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Exit Saving Changes

After making your selections on the Setup menus, always select "Exit Saving Changes". This procedures stores the selections displayed in the menus in CMOS (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.
If you attempt to exit without saving, the program asks if you want to save before exiting. During boot-up, Phoenix BIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu.
If, during boot-up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.
Press <F1> to resume the boot or <F2> to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.
Selecting "Discard Changes" on the Exit menu updates all the selections with their previous values.

Save Changes

Selecting "Save Changes" saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

5.3 BIOS and Firmware Update

If a System-BIOS and Microcontroller Firmware update is required please follow these instructions:

Firmware update:

1.) Create a bootable DOS disk, USB-stick or hard disk.

2.) Copy the directories \BIOS and \Firmware to this device.

3.) Boot the system from this device.

4.) Change to the directory \Firmware

5.) Type "ecupdate" to update the System Firmware.

6.) When the Firmware update has finished, the system switches off automatically.

Note: Depending on how old the previous Firmware version was, the Firmware update may well fail on the first attempt (board reboots or turns off without any update) In this case simply repeat the procedures 3 – 6 above.

BIOS update:

1. to 3.) see above

4.) Change to the directory \BIOS

5.) Type "update" to update the System BIOS.

6.) When the BIOS update has finished, reboot the system.

Note: After the system has been updated, the CMOS has been changed to defaults and therefore it is necessary to enter Setup (press F2 at boot time) to configure the system settings.

5.4 Bios Crisis Recovery

Should the BIOS setup be altered, such that it is no longer possible to re-enter the BIOS setup – for example if wrong display selected, the following methods can be used to restore the default settings:

1. Blind reset to defaults
2. Crisis recovery / clear backup EEPROM jumper
3. Crisis recovery software (usually only necessary if the BIOS is corrupted – for example if power was removed during a BIOS update)

1. Blind Reset to defaults

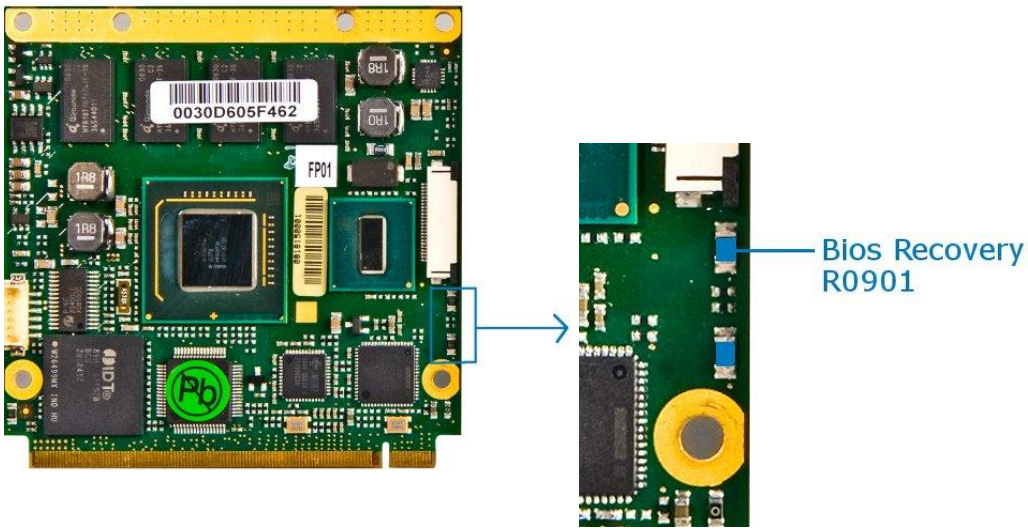
In the event that there is no display or the display is for some reason not active, in order to get the BIOS back to the default settings (and so enable the display) the following sequence must be performed:

1. During boot press F2 to get into BIOS setup (F2 can be pressed repeatedly, at least until the Numlock LED on Keyboard is on)
2. Press F9 and then enter to reset to default settings
3. Press F10 and then enter to save and exit the BIOS setup
4. System should then reboot with the default settings.

2. Crisis Recovery / Clear backup EEPROM Jumper

The two pads of R0901 should be shorted (using tweezers or pliers) before applying power to the board and held shorted until the crisis recovery has started. As soon as crisis recovery is started the short can be removed.

Note: ***R0901 is connected to +3,3V so be highly aware that the tweezers do not touch the heat spreader or any other electronic component on the board. The board could otherwise be damaged.***



3. Crisis Recovery software

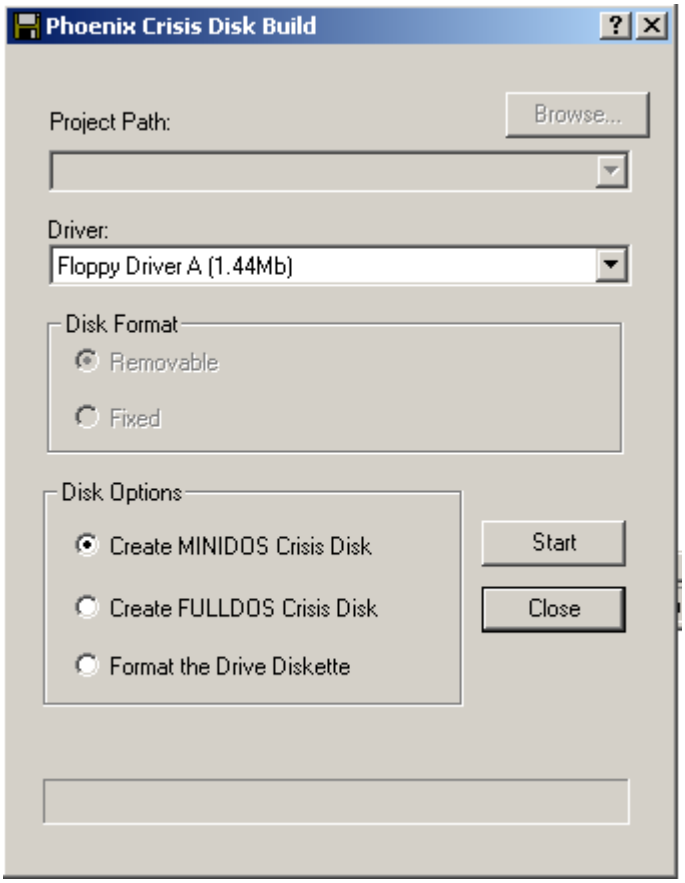
This technique should only be required in the event of a serious corruption of the BIOS – for example following an unsuccessful attempt to update the BIOS

To use this technique a special software - CRISDISK - and a USB dongle must be obtained from MSC.

Note: Contact the MSC customer support for information how to obtain the CRISDISK.ZIP software and the USB recovery dongle.

Please follow these simple steps to create a bootable crisis recovery medium:

1. Unzip CRISDISK.ZIP and start the windows-based program WINCRIS.EXE on the host system. A window will pop up as shown below:



2. In the drop-down box, select either "Floppy Drive A" to create a recovery disk, or select "Removable Disk 0 (xxx Mb)" to create a recovery USB stick. Disk options should be left as "Create MINIDOS Crisis Disk".

3. Press the start button to generate the selected crisis recovery medium.

Proceed as follows to use the generated Disk or USB stick for the recovery:

Plug the USB dongle into a free USB port on the failing system before switching the system on. Please make sure that you use different USB controllers for USB dongle and USB crisis recovery medium. After power-up, crisis recovery mode should start automatically.

The programming process is signalled by short beeps and terminated after successful programming with one long beep. After that, the system is automatically rebooted.

Important Notes:

- USB recovery dongle and USB crisis recovery device must not be plugged to the same USB controller.
- Crisis recovery may take up to 5 minutes
- A long beep indicated successful recovery
- Crisis recovery does not include the boot block.

5.5 Diagnostics Postcodes

Postcodes can be seen on a special Postcode display, either on the MSC mainboard or on an external Postcode PCI card. There is an item in the bios setup to select the bus that should get the postcode data: either PCI (for external cards) or LPC (for onboard displays).

If a postcode display has only 2 digits, only the lower byte of word-value postcodes will be shown.

5.5.1 Bootblock Bios Postcodes

Code	Bootblock Task Description
BBH	Bootblock Early Init after Reset
80h	Chipset Init
81h	Bridge Init
82h	CPU Init
83h	System Timer Init
84h	System I/O Init
85h	Check forced Recovery Boot, CMOS & CMOS Backup Clear
86h	Check BIOS Checksum
87h	Goto BIOS, start early BIOS initialzations
88h	Init Multi Processor
89h	Set Huge Segment
8Ah	OEM Initializations
8Bh	Init Interrupt and DMA Controller
8Ch	Init Memory Type
8Dh	Init Memory Size
8Eh	Shadow Boot Block
8Fh	Init SMM
90h	System Memory Test
91h	Init Interrupt Vectors
92h	Init Realtime Clock
93h	Init Standard Video
94h	Init Beeper
95h	Initialize USB Controller
95h	Init Boot
96h	Clear Huge Segment
97h	Boot OS
99h	Init Security

5.5.2 System Bios Postcodes

Code	Beeps	POST Task Description
04h		Get CPU type
03h		Disable Non-Maskable Interrupt (NMI)
06h		Initialize system hardware
07h		Disable shadow and execute code from the ROM.
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize fixed disk drives
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 kB Base RAM
2Ch	1-3-4-1	RAM Address test
2Eh	1-3-4-3	Base RAM Test
2Fh		Enable cache before system BIOS shadow
32h		Compute CPU clock speed in MHz
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
41h		Initialize RomPilot
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
47h		Initialize I20 support
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Initialize MultiBoot
50h		Display CPU type and speed

Code	Beeps	POST Task Description
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled
55h		Configure USB devices
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Disable CPU cache
5Ch		Conventional memory test
60h		Extended memory test
62h		Address Test on Extended Memory
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		CPU feature, MP, and APIC initialization
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display BIOS shadow status
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		Initialilze Intelligent System Monitoring
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialisation
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports.
87h		Configure Motheboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Program timing registers according to PIO modes
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1-2	Enable PCI devices and ROM Scan One long, two short beeps on checksum failure
99h		Check for SMART Drive
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives

Code	Beeps	POST Task Description
A0h		Set time of day
A2h		Check key lock
A4h		Initialize typematic rate
A8h		Erase F2 prompt
AAh		Scan for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B1h		Inform RomPilot about the end of POST.
B2h		POST done - prepare to boot operating system
B3h		store enhanced CMOS values in non-volatile area
B4h		1 One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B7h		Initialize ACPI BIOS
B9h		Prepare Boot
BAh		Initialize DMI parameters
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and backup reminders
C0h		Try to boot with INT 19
C1h		Initialize POST PEM Error Manager
C2h		Initialize PEM error logging
C3h		Initialize error PEM display function
C4h		Initialize PEM system error handler
C5h		PnPnd dual CMOS (optional)
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
CAh		Redirect Int 15h to enable remote keyboard
CBh		Redirect Int 13h to Memory Technologies
CCh		Redirect Int 10h to enable remote serial video
CDh		Remap I/O and memory for PCMCIA
CEh		Initialize digitizer and display message
D2h		Unknown interrupt or exception

5.5.3 Memory Detection Postcodes

Code	Calistoga Memory Detection
FFA0h	Start memory detection
FF01h	Enable MCHBAR
FF02h	Check for DRAM initialisation interrupt and reset fail
FF03h	Verify all DIMMs are DDR2 and unbuffered
FF04h	Detect an improper warm reset and handle
FF05h	Detect if ECC SO-DIMMs are present in the system
FF06h	Verify all DIMMs are single or double sided and not asymmetric
FF07h	Verify all DIMMs are x8 or x16 width
FF08h	Find a common CAS latency between the DIMMS and the MCH
FF09h	Determine the memory frequency and CAS latency to program
FF10h	Determine the smallest common TRAS for all DIMMs
FF11h	Determine the smallest common TRP for all DIMMs
FF12h	Determine the smallest common TRCD for all DIMMs
FF13h	Determine the smallest refresh period for all DIMMs
FF14h	Verify burst length of 8 is supported by all DIMMs
FF15h	Determine the smallest tWR supported by all DIMMs
FF16h	Determine DIMM size parameters
FF17h	Program Graphics frequency and PLL settings
FF18h	Program system memory frequency
FF19h	Determine and set the mode of operation for the memory channels
FF20h	Program clock crossing registers
FF21h	Disable Fast Dispatch
FF22h	Program the DRAM Row Attributes and DRAM Row Boundary registers
FF23h	Program the DRAM Bank Architecture register
FF24h	Program the DRAM Timing & and DRAM Control registers
FF25h	Program ODT
FF26h	Perform steps required before memory init
FF27h	Program the receive enable reference timing control register Program the DLL Timing Control Registers , RCOMP settings
FF28h	Enable DRAM Channel I/O Buffers
FF29h	Enable all clocks on populated rows
FF30h	Perform JEDEC memory initialization for all memory rows
FF31h	Program PM Settings
FF32h	Perform additional steps required after memory init
FF33h	Program DRAM throttling and throttling event registers
FF34h	Setup DRAM control register for normal operation and enable
FF35h	Setup DRAM control register for normal operation and enable
FF36h	Enable RCOMP
FF37h	Clear DRAM initialization bit in the ICH

5.5.4 ACPI Postcodes

Code	ACPI Codes
03h	Enter Suspend State S3
04h	Enter Hibernate State S4
05h	Enter Softoff State S5
ABh	Enter Wakeup from Powerstate
CDh	End Wakeup from Powerstate